REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Final Office Action dated November 3, 2006, has been received and its contents carefully reviewed.

No claims are hereby amended. No claims are hereby canceled and no claims are hereby added. Accordingly, claims 1-30 are currently pending. Reexamination and reconsideration of the pending claims is respectfully requested.

In the Office Action, claims 1-30 are rejected under 35 U.S.C. §103(a) as allegedly unpatentable over WO 03/058332 A1 (to Lee et al.)(hereinafter "Lee").

The rejection of claims 1-7 is respectfully traversed and reconsideration is requested. Claims 1-7 are allowable over the cited reference in that each of these claims recite a combination of elements including, for example, " ... a first gate redundancy line formed on the interlayer insulating layer, and connected electrically with just one of the gate electrodes, one of the gate lines, and both gate electrode and gate line through a first gate contact hole and formed of the same material as one of the source and drain electrodes ... a pixel electrode electrically connected with the drain electrode through the drain contact hole formed in the passivation layer." Lee does not teach or suggest at least these features of the claimed invention.

In rejecting claim 1, the Examiner equates Lee's reference number 170 with that of Applicant's first gate redundancy line. The Examiner equates Lee's reference number 175 with that of Applicant's second gate redundancy line. However, Lee's reference number 170 refers to *a gate pad electrode* and 175 refers to a *pad contact hole*. Clearly, the Lee elements identified by the Examiner are not those as claimed by Applicant. In addition, the Examiner did not address at least the claimed limitation, "a first gate redundancy line formed on the interlayer insulating layer, and connected electrically with just one of the gate electrodes, one of the gate lines, and both gate electrode and gate line through a first gate contact hole." Furthermore, the Examiner states that, "Lee et al., however, do not disclose the first gate redundancy line being formed of the same material as one of the source and drain electrode. It would have been obvious to one skilled in the art at the time of the invention was mad [sic] to form a gate redundancy electrode and source/drain electrode having a same based material, since it is a common practice in the art to simplify process steps for forming an LCD device." (Office Action at page 3). The Examiner's

taking what appears to be Official Notice is seasonably traversed and objected to by Applicants. There may be other reasons for forming a gate redundancy line of the same material as source and drain electrodes other than those reasons provided by the Examiner. For example, choice of materials for redundancy lines and source and drain electrodes may be a function of line resistance and signal delay. If the Examiner maintains the Examiner's rejection, Applicants request that the Examiner provide documents to support the Examiner's basis for rejection. Furthermore, Applicants respectfully note that the Examiner did not address the limitation, "a pixel electrode electrically connected with the drain electrode through the drain contact hole formed in the passivation layer." Accordingly, claim 1 and claims 2-7, which depend either directly or indirectly on claim 1, are allowable over the Lee reference.

The rejection of claims 8-13 is respectfully traversed and reconsideration is requested. Claims 8-13 are allowable over the cited reference in that each of these claims recite a combination of elements including, for example, " ... a pixel electrode electrically connected with the drain electrode through a drain contact hole formed in the passivation layer; and a gate redundancy line formed on the passivation layer, and connected electrically with just one of the gate electrodes, the gate lines, and both gate electrode and gate line through a gate contact hole and formed of the same material as the pixel electrode." Lee does not teach or suggest at least these features of the claimed invention.

Applicants first respectfully point out that the Examiner did not address any of the above claimed elements in the Examiner's rejection of at least claim 8. Furthermore, Applicants' arguments with respect to the rejection of claims 1-7 apply equally to the rejection of claims 8-13 and will thus not be repeated herein. Accordingly, claim 8 and claims 9-13, which depend either directly or indirectly on claim 8, are allowable over the Lee reference.

The rejection of claims 14-23 is respectfully traversed and reconsideration is requested. Claims 14-23 are allowable over the cited reference in that each of these claims recite a combination of elements including, for example, " ... forming a first gate redundancy line on the interlayer insulating layer electrically connected with just one of the gate electrodes, the gate lines, and both the gate electrode and gate line through a first gate contact hole ... forming a drain contact hole in the passivation layer, and forming a pixel electrode connected electrically with the drain electrode through the drain contact hole." Lee does not teach or suggest at least these features of the claimed invention.

Applicants' arguments with respect to the rejection of claims 1-13 apply equally to the rejection of claims 14-23 and will thus not be repeated herein. Accordingly, claim 14 and claims 15-23, which depend either directly or indirectly on claim 14, are allowable over the Lee reference.

The rejection of claims 24-30 is respectfully traversed and reconsideration is requested. Claims 24-30 are allowable over the cited reference in that each of these claims recite a combination of elements including, for example, " ... forming a gate contact hole in the passivation layer, and forming a gate redundancy line connected electrically with just one of the gate electrodes, the gate lines, and both gate electrode and gate line through the gate contact hole." Lee does not teach or suggest at least these features of the claimed invention.

Applicants' arguments with respect to the rejection of claims 1-23 apply equally to the rejection of claims 24-30 and will thus not be repeated herein. Accordingly, claim 24 and claims 25-30, which depend either directly or indirectly on claim 24, are allowable over the Lee reference.

Applicants furthermore seasonably traverse and object to the Examiner's taking Official Notice with respect to the rejection of claims 2, 9, 16 and 26 (Office Action at page 3). In rejecting claims 2, 9, 16 and 26, the Examiner states, "although Lee et al. do not explicitly disclose a top gate type TFT, it would have been an obvious to one having ordinary skill in the art at the time the invention was made to employ the Lee et al device having a top gate TFT since the examiner takes Office Notice of the equivalence of a top gate type TFT and a bottom type TFT for their use in the display art and the selection of any of these known equivalents to operate a display device would be within the level of ordinary skill in the art." (Office Action at page 3). Applicants respectfully note that top gate and bottom gate TFTs are manufactured by very different processes. At least claims 16, 18, 26 and 28 are method claims claiming the fabrication method of an array substrate in either top or bottom gate TFT *manner*. That is, these claims are not just device limitations but require a *manner* of formation. Accordingly, the Examiner's taking of Official Notice is inappropriate.

Applicants respectfully request that the Examiner withdraw Finality at least for all of the above reasons.

Applicants believe the foregoing remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Dated: March 5, 2007

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